AMENDMENTS TO THE SPECIFICATION

After the title, before the first line, please insert the following:

--This application is a divisional of Application Serial No. 10/424,086 filed April 28, 2003, which is a divisional of Application Serial No. 09/989,155, filed November 21, 2001.--

Please amend the third paragraph on page 66, as follows:

Two-input NAND gates 161 whose inputs are the memory cell array selecting line 170 and the main bit line 167 are connected at intersections of a plurality of memory cell array selecting lines 170 and a plurality of main bit lines ~~67~~ 167, and outputs thereof are connected to sub-bit lines 164 through the column read/write first control circuit CRW1. The sub-bit lines 164 correspond to the bit lines of each MRAM cell array 166.

Please amend the formula on page 3, line 7, of the specification as follows:

~~$$TMRR = \frac{R_{AF} - R_F}{R_A} = \frac{P_1 P_2}{1 - P_1 P_2}$$~~

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